T Number	Ti ba	Coarch Tout	l pp	Time stamp
L Number	Hits 3		USPAT	2003/05/07 16:28
1 -	18		USPAT;	2003/05/06 11:15
-	10	WILLIAMS-ANTHONY-D WILLIAMS-ANTHONY).in.	EPO; JPO;	2003/03/06 11:13
		WIDDIANS-ANTHONI-D WIDDIANS-ANTHONI).III.	IBM TDB	
_	11	(seltzer fulton patel-dhimant	USPAT;	2003/05/02 15:43
-	**	kumar-veena).in. and xilinx.as.	EPO; JPO;	2003/03/02 13.43
		Admid Veenay. In. and XIIIIX. as.	IBM TDB	
	1	6002861.pn.	USPAT;	2003/05/02 15:56
İ	_		EPO; JPO;	2003,03,02 13.30
			IBM TDB	
_	1	"4697241".PN.	USPAT	2003/05/02 21:00
_	1		USPAT	2003/05/02 15:56
-	1	"4775950".PN.	USPAT	2003/05/02 15:56
_		703/16.ccls.	USPAT;	2003/05/02 15:56
			EPO; JPO;	
			IBM TDB	
-	28723	(hardware same logic same simulator) or	USPAT;	2003/05/02 21:15
		(VHDL or HDL or (schematic adj c) or ASIC or	JPO;	
		FPGA)	DERWENT;	
			IBM TDB	1
-	11381	((hardware same logic same simulator) or	USPAT;	2003/05/02 21:17
		(VHDL or HDL or (schematic adj c) or ASIC or	JPO;	
		FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)	IBM_TDB	
-	11104	' ' '	USPAT;	2003/05/02 21:17
		(VHDL or HDL or (schematic adj c) or ASIC or	JPO;	
		FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)) and	IBM_TDB	
		(documentation or description or		
1		recommendation)		
-	2840	' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' ' '	USPAT;	2003/05/02 21:17
		(VHDL or HDL or (schematic adj c) or ASIC or	JPO;	
		FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)) and	IBM_TDB	
		(documentation or description or		
		recommendation)) and ((design adj module) or		
		(design adj element) or (core) or (IP) or		
	687	((intellectual adj property)) (((((hardware same logic same simulator) or	IICDAM.	2003/05/02 21:17
-	007	(VHDL or HDL or (schematic adj c) or ASIC or	USPAT; JPO;	2003/05/02 21:1/
		FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)) and	IBM_TDB	
		(documentation or description or	12123	
		recommendation)) and ((design adj module) or		1
		(design adj element) or (core) or (IP) or		
		(intellectual adj property))) and (hierarchy		
		or hierarchical)		
-	621	l '	USPAT;	2003/05/02 21:18
		(VHDL or HDL or (schematic adj c) or ASIC or	JPO;	
		FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)) and	IBM_TDB	
		(documentation or description or		
		recommendation)) and ((design adj module) or		
		(design adj element) or (core) or (IP) or		
1		(intellectual adj property))) and (hierarchy		
1		or hierarchical)) and (store or storage or		
		database)		
] -	243	· · · · · · · · · · · · · · · · · · ·	USPAT;	2003/05/02 21:18
		or (VHDL or HDL or (schematic adj c) or ASIC	JPO;	
		or FPGA) ) and (convert or conversion or	DERWENT;	
		translate or translation)) and	IBM_TDB	İ
		(documentation or description or		]
		recommendation)) and ((design adj module) or (design adj element) or (core) or (IP) or		
		(intellectual adj property))) and (hierarchy		]
]		or hierarchical)) and (store or storage or		
j l		database)) and (debug or debugging)		
<u> </u>	423	(VHDL or HDL or (schematic adj c)) and (ASIC	USPAT;	2003/05/02 21:17
	123	or FPGA) and ((hardware same simulat\$3) or	JPO;	-003,03,02 21.11
[ ]		(logic same simulat\$3))	DERWENT;	
		1,10310 04111414040///	IBM TDB	
<u></u>				

		_		
-	274	' '   '   '   '   '   '   '   '   '	USPAT;	2003/05/02 21:17
		(ASIC or FPGA) and ((hardware same	JPO;	
1		simulat\$3) or (logic same simulat\$3)) ) and	DERWENT;	
		(convert or conversion or translate or translation)	IBM_TDB	
1_	274	(((VHDL or HDL or (schematic adj c)) and	IICDAM.	2002/05/02 21 12
	2/4	(ASIC or FPGA) and ((hardware same	USPAT; JPO;	2003/05/02 21:17
		simulat\$3) or (logic same simulat\$3)) ) and	DERWENT;	İ
		(convert or conversion or translate or	IBM TDB	
		translation)) and (documentation or	15.1100	
		description or recommendation)		
-	145	((((VHDL or HDL or (schematic adj c)) and	USPAT;	2003/05/02 21:30
1		(ASIC or FPGA) and ((hardware same	JPO;	,,
	]	simulat\$3) or (logic same simulat\$3)) ) and	DERWENT;	1
		(convert or conversion or translate or	IBM TDB	
		translation)) and (documentation or	_	
		description or recommendation)) and ((design		
		adj module) or (design adj element) or		<b>-</b>
		(core) or (IP) or (intellectual adj		-
		property))		
-	103	· · · · ·	USPAT;	2003/05/02 21:29
		(ASIC or FPGA) and ((hardware same simulat\$3)) ) and	JPO;	
		(convert or conversion or translate or	DERWENT;	
	1	translation)) and (documentation or	IBM_TDB	
		description or recommendation)) and ((design		
		adj module) or (design adj element) or		
		(core) or (IP) or (intellectual adj		i
		property))) and (hierarchy or hierarchical)		
-	100	((((((VHDL or HDL or (schematic adj c)) and	USPAT;	2003/05/02 21:18
	i	(ASIC or FPGA) and ((hardware same	JPO;	2005, 05, 02 22, 25
		simulat\$3) or (logic same simulat\$3)) ) and	DERWENT;	!
	•	(convert or conversion or translate or	IBM_TDB	
		translation)) and (documentation or	_	
		description or recommendation)) and ((design		
		adj module) or (design adj element) or		
		(core) or (IP) or (intellectual adj		
	i	property))) and (hierarchy or hierarchical))	İ	
	72	<pre>and (store or storage or database) (((((((VHDL or HDL or (schematic adj c)) and</pre>	HODAM	0000/05/00 01 10
	/2	(ASIC or FPGA) and ((hardware same	USPAT; JPO;	2003/05/02 21:19
		simulat\$3) or (logic same simulat\$3)) ) and	DERWENT;	
		(convert or conversion or translate or	IBM TDB	
1		translation)) and (documentation or		
		description or recommendation)) and ((design		
		adj module) or (design adj element) or		
		(core) or (IP) or (intellectual adj		
		<pre>property))) and (hierarchy or hierarchical))</pre>		
		and (store or storage or database)) and		
		(debug or debugging or (error same (detect\$3		
_	72	or locat\$3 or find\$3)))		0000/0=/:-
-	/2		USPAT;	2003/05/02 21:29
		<pre>and (ASIC or FPGA) and ((hardware same simulat\$3) or (logic same simulat\$3)) ) and</pre>	JPO;	ļ
		(convert or conversion or translate or	DERWENT; IBM_TDB	
		translation)) and (documentation or	1 TEM_1 DB	
		description or recommendation)) and ((design		
	,	adj module) or (design adj element) or		
		(core) or (IP) or (intellectual adj		
]		<pre>property))) and (hierarchy or hierarchical))</pre>		
		and (store or storage or database)) and		
		(debug or debugging or (error same (detect\$3		
]		or locat\$3 or find\$3)))) and (link\$3 or		
		connect\$3 or associat\$3)		

-	145	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)) or (logic same simulat\$3)) ) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:31
	0	((((VHDL or HDL or (schematic adj c)) and (ASIC or FPGA) and ((hardware same simulat\$3)) or (logic same simulat\$3))) and (convert or conversion or translate or translation)) and (documentation or description or recommendation)) and (((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same ((design adj module) or (design adj element) or (core) or (IP) or (intellectual adj property)) same (link\$3 or connect\$3 or associat\$3) same (simulation with (result or data or info or information or vector)))	USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:34
-	2		USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:35
	6		USPAT; JPO; DERWENT; IBM_TDB	2003/05/02 21:38
-			USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:08
-	102	(VHDL) and (nigh adj level) and (physical adj implementation)	USPAT; JPO; DERWENT; IBM_TDB	2003/05/05 10:10

_	0	(VHDL) and ((high adj level) same (physical adj implementation)) same ((data adj base)	USPAT; JPO;	2003/05/05 10:11
		or (database))	DERWENT;	
			IBM TDB	
_	77	(	USPAT;	2003/05/05 10:11
		adj implementation)) and database	JPO;	
			DERWENT;	
			IBM_TDB	
-	2	(((VHDL) and (high adj level) and (physical	USPAT;	2003/05/05 10:11
		adj implementation)) and database) and	JPO;	l
		testbench	DERWENT;	
			IBM_TDB	
-	3	object same oriented same VHDL same database	USPAT;	2003/05/06 13:43
			EPO; JPO;	
			IBM_TDB	
-	223	(rostocher).in. OR (dangelo).in.	USPAT;	2003/05/06 13:45
			EPO; JPO;	
			IBM_TDB	
-	8	(hierarch\$4 or generation\$2 or tree or	USPAT;	2003/05/06 13:45
		child\$3) same VHDL same database	EPO; JPO;	
			IBM_TDB	